AMENDMENTS TO THE DRAWINGS

(1) The Examiner objected to the drawings under 37 CFR 1.83(a) for failing to show test fixture 42. The paragraph beginning on page 4, line 13 of the specification has been amended to replace reference numeral 42 with reference numeral 10. Therefore the objection is believed to be moot.

(2) The Examiner objected to the drawings under 37 CFR 1.83(a) for failing to show a tester. FIG. 4 has been amended to show tester 250 and the paragraph beginning on page 6, line 7 of the specification has been amended to introduce the reference number 250 for the previously mentioned tester. Therefore the objection is believed to be moot.

(3) The Examiner objected to the drawings because multiple holes on PCB 210 for connector 220 requires a reference numeral. FIG. 4 has been amended to label the holes with reference numeral 203 and the paragraph beginning on page 6, line 7 of the specification has been amended to introduce the reference number 203 for the previously mentioned holes. Therefore the objection is believed to be moot.

(4) The Examiner objected to the drawings because multiple electrical pads of second interface 204 requires a reference numeral. FIG. 4 has been amended to label the electrical pads with reference numeral 205 and the paragraph beginning on page 6, line 11 of the specification has been amended to introduce the reference number 205 for the previously mentioned electrical pads. Therefore the objection is believed to be moot.

(5) The Examiner objected to the drawings because various nodes on PLC requires a reference numeral. FIG. 4 has been amended to label the nodes with reference numeral 232 and the paragraph beginning on page 6, line 11 of the specification has been amended to introduce the reference number 232 for the previously mentioned nodes. Therefore the objection is believed to be moot.

(6) The Examiner objected to the drawings because wire bonding between 210 and 230 requires a reference numeral. FIG. 4 has been amended to label the illustrated wirebonding with reference numeral 234 and the paragraph beginning on page 6, line 11 of the specification has been amended to introduce the reference number 234 for the previously mentioned wirebonding. Therefore the objection is believed to be moot.

(7) The Examiner objected to the drawings because the soldering wires of claim 3 are allegedly not shown. Applicants respectfully disagree. The wires were shown in FIG. 4 and have now been labeled wirebonds 234. Therefore the objection is believed to be moot.

REMARKS

Claims 1-7 remain in this application. Claims 8-18 have been cancelled without prejudice to their subsequent reinstatement due to the restriction requirement. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §121 Election/Restrictions

The Patent Office has issued a restriction under 35 U.S.C. § 121 to one of the following inventions:

I. Claims 1-7, drawn to method of optically and electrically testing a planar lightwave circuit, classified in class 324, subclass 158.1;

II. Claims 8-12, drawn to a test fixture, classified in class 324, subclass 754; and

III. Claims 13-18, drawn to a test fixture, classified in class 324, subclass 765.

In response to the restriction, the Applicant hereby affirm the election without traverse to prosecute the claims of Group I (that is claims 1-7). Claims 8-18 have been canceled herein without prejudice to their reinstatement in one or more other applications.

35 U.S.C. §102(e) Rejection - Levy

The Examiner has rejected claim 1 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. (6,535,659) issued to Levy (hereinafter referred to as "Levy").

As an initial matter, Levy may not represent effective prior art to the present application because of Applicant's early date of invention. However, while making this

statement, and reserving the right to swear behind Levy in the future, the Applicant chooses at this time to present arguments pointing out certain differences between claim 1 and the disclosure of Levy.

Claim 1 recites "*A method of electrically and optically testing a planar lightwave circuit comprising: placing the planar lightwave circuit on a test fixture the test fixture including a printed circuit board; electrically coupling the printed circuit board to the planar lightwave circuit; electrically coupling the printed circuit board to a tester;* ***optically coupling the planar lightwave circuit to the tester****; and performing electrical and* ***optical*** *testing on the planar lightwave circuit*". Levy does not teach or reasonably suggest these limitations.

In particular, Levy does not teach or reasonably suggest either: (a) optically coupling the planar lightwave circuit to the tester; or (b) optically testing the planar lightwave circuit. Levy discusses electrically testing waveguide array units (see for example the Field of the Invention). Levy discusses that the waveguide array units may be electrically tested for shorts between waveguides and for shorts between waveguides and the substrate (see for example column 1, lines 61-66).

In the Office Action, the Examiner stated that Levy teaches optically coupling the planar lightwave circuit to the tester at column 1, lines 17-48 (see page 7). Applicants respectfully disagree. Column 1, lines 17-48 refer primarily to FIG. 1, which shows an integrated optical interconnect unit 10 employing a waveguide array structure. There is absolutely no teaching or suggest that the integrated optical interconnect unit 10 is used to test the waveguide array structure. As understood by Applicants, if the waveguide array structure is going to be tested, it would need to be tested before inclusion in the integrated optical interconnect unit 10. Aside from FIG. 1, Levy does not teach or

reasonably suggest optically coupling the waveguide array structure, at least not for the purposes of optical testing.

Accordingly, Levy does not teach or reasonably suggest either: (a) optically coupling the planar lightwave circuit to the tester; or (b) optically testing the planar lightwave circuit.

Anticipation under 35 U.S.C. Section 102 requires every element of the claimed invention be identically shown in a single prior art reference. The Federal Circuit has indicated that the standard for measuring lack of novelty by anticipation is **strict identity**. "*For a prior art reference to anticipate in terms of 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference.*" *In Re Bond*, 910 F.2d 831, 15 USPQ.2d 1566 (Fed. Cir. 1990).

For at least these reasons, **claim 1** is believed to be allowable over Levy. **Claims 2-7** depend from **claim 1** and are believed to be allowable therefor, as well as for the recitations independently set forth therein.

35 U.S.C. §103(a) Rejection – Levy in view of Forsyth

The Examiner has rejected claims 2-7 under 35 U.S.C. §103(a) as being unpatentable over Levy as applied to claim 1 above, and further in view of U.S. Patent No. 4,910,548 issued to Forsyth et al. (hereinafter "Forsyth").

Firstly, Applicants do not think that it is appropriate to combine Levy and Forsyth. Applicants may elect at a later date to argue formally that Levy and Forsyth should not be combined.

Secondly, the combination of Levy and Forsyth proposed by the Examiner does not teach or suggest all of the limitations of **claim 1**. Any combination of Levy and

Forsyth does not disclose optically coupling a planar lightwave circuit to a tester and performing optical testing on the planar lightwave circuit. As discussed above, Levy does not discuss optical testing. Forsyth does not teach or reasonably suggest that the device under test is a planar lightwave circuit.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest **all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Accordingly, **claim 1** and its dependent **claims 2-7** are believed to be allowable over Levy and Forsyth.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 4-18-05

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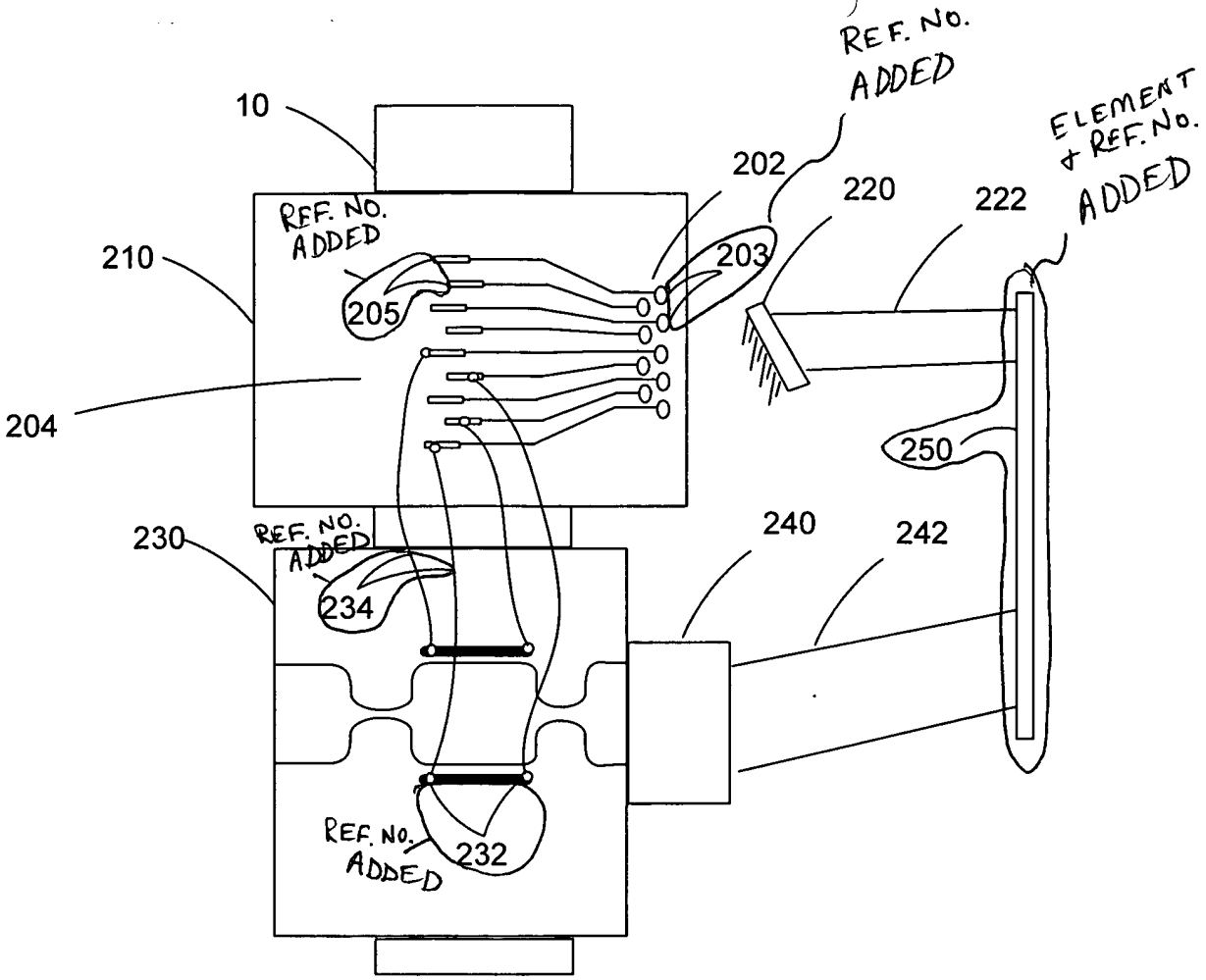

FIG. 4